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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,651	09/19/2003	Jae Hun Ku	AMKOR-041G	6079

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,651	KU ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 17-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 17-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/29/03;1/2/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 17-26 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,573,123 to Li et al.

Regarding claim 17, Li et al. (figures 2-12) teach a method for fabricating a semiconductor package, comprising:

placing a lead frame (222) which defines a space (a space is between the lead frame [222] and the chip [210]) for accommodating a semiconductor chip (210) and includes a plurality of leads (222) which each have a bottom surface onto an adhesive tape (250);

placing a semiconductor chip (210) having a bottom surface (a bottom surface of chip [210]) and a plurality of bond pads (212) onto the adhesive tape (250) within the space defined by the lead frame;

electrically connecting at least one of the bond pads (212) of the semiconductor chip (210) to one of the leads (222);

at least partially encapsulating the semiconductor chip (210) and the leads (222) with an encapsulant material (240) to form a package body; and

removing the adhesive tape (250) from the package body such that the bottom surface of each of the leads (222) and the bottom surface of the semiconductor chip (210) are exposed in the package body.

Regarding claim 18, Li et al. teach removing portions of the lead frame (222), which protrudes from the package body from the semiconductor package.

Regarding claim 19, Li et al. inherent teach applying pressure to the lead frame (222) and to the semiconductor chip (210) to firmly affix the lead frame (222) and the semiconductor chip (210) to the adhesive tape (250).

Regarding claim 20, Li et al. teach electrically connecting the bond pads (212) of the semiconductor chip (210) to respective ones of the leads (222) via conductive wires (230); and encapsulating the wires (230) with the encapsulant material (240).

Regarding claim 21, Li et al. teach partially encapsulating (240) the leads (222) such that an outer end (an outer portion of leads [222]) of each of the leads (222) is exposed in the package body.

Regarding claim 22, Li et al. (figures 2-12) a method of fabricating a semiconductor package, comprising:

placing a lead frame (222) defining a space (a space is between the lead frame [222] and the chip [210]) for accommodating a semiconductor chip (210) and including a ground ring (a portion of window pad [224], column 1, lines 41-43) which has a bottom surface (a bottom surface of [224]) and a plurality of leads (222) which each have a bottom surface (a bottom surface of leads [222]) onto an adhesive tape (250);

placing a semiconductor chip (210) having a bottom surface (a bottom surface of chip [210]) and a plurality of bond pads (212) onto the adhesive tape (250) within the space defined by the lead frame (222);

electrically connecting at least one of the bond pads (212) of the semiconductor chip (210) to one of the leads (222) and at least one of the bond pads (212) to the ground ring (a portion of window pad [224]);

at least partially encapsulating the semiconductor chip (210), the ground ring (a portion of window pad [224]), and the leads (222) with an encapsulant material (240) to form a package body; and

removing the adhesive tape (250) from the package body such that the bottom surface of each of the leads (222), the bottom surface of the ground ring (a portion of window pad [224]), and the bottom surface of the semiconductor chip (210) are exposed in the package body.

Regarding claim 23, Li et al. teach removing portions of the lead frame (222), which protrude from the package body from the semiconductor package.

Regarding claim 24, Li et al. inherent teach applying pressure to the lead frame (222) and to the semiconductor chip (210) to firmly affix the lead frame (222) and the semiconductor chip (210) to the adhesive tape (250).

Regarding claim 25, Li et al. teach electrically connecting the bond pads (212) of the semiconductor chip (210) to respective ones of the leads (222) via conductive wires (230); and encapsulating the wires (230) with the encapsulant material (240).

Regarding claim 26, Li et al. teach partially encapsulating (240) the leads (222) such that an outer end (an outer portion of leads [222]) of each of the leads (222) is exposed in the package body.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 27-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,573,123 to Li et al. in view of US Patent No. 6,081,029 to Yamaguchi.

Regarding claim 27, Li et al. (figures 2-12) teach a method for fabricating a semiconductor package, comprising:

a plurality of leads (222) which each have a bottom surface (a bottom surface of leads [222]) onto an adhesive tape (250);

attaching a semiconductor chip (210) having a plurality of bond pads (212);

electrically connecting at least one of the bond pads (212) of the semiconductor chip (210) to one of the leads (222);

at least partially encapsulating the semiconductor chip (210), the leads (222) with an encapsulant material (240) to form a package body; and

removing the adhesive tape (250) from the package body such that the bottom surface of each of the leads (222) is exposed in the package body.

Li et al. differ from the claimed invention by not showing placing a chip paddle. However, Yamaguchi (figures 1-6) teaches a chip paddle (13). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yamaguchi into the device taught by Li et al. because it is used for supporting the semiconductor chip. The combined device shows placing a lead frame including a chip paddle having a bottom surface and removing the adhesive tape from the package body such that the bottom surface of the chip paddle is exposed in the package body.

Regarding claim 28, the combined device shows removing portions of the lead frame (Li et al.; 222), which protrude from the package body from the semiconductor package.

Regarding claim 29, the combined device inherent teaches applying pressure to the lead frame (Li et al.; 222) to firmly affix the lead frame to the adhesive tape (Li et al.; 250).

Regarding claim 30, the combined device shows electrically connecting the bond pads (Li et al.; 212) of the semiconductor chip (Li et al.; 210) to respective ones of the leads (Li et al.; 222) via conductive wires (Li et al.; 230); and encapsulating the wires (Li et al.; 230) with the encapsulant material (Li et al.; 240).

Regarding claim 31, the combined device shows partially encapsulating (Li et al.; 240) the leads (Li et al.; 222) such that an outer end (Li et al.; an outer portion of leads [222]) of each of the leads (Li et al.; 222) is exposed in the package body.

Regarding claim 32, the combined device shows attaching the semiconductor chip (Yamaguchi; 15) to the chip paddle (Yamaguchi; 13) via an adhesive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
June 08, 2004

Sara Crane
Primary Examiner